The Application Benefit of X-series 6.5kV/900A HVIGBT for Rolling Stock

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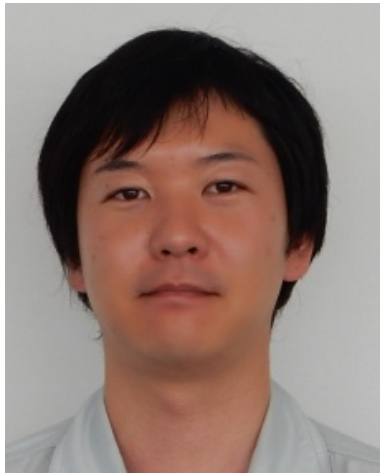

OUTLINE

1. Introduction
2. Chip technologies
3. Application benefit
4. Conclusion

Introduction(Product features)

Traction

large amounts of energy

HVIGBT module
CM900HG-130X(6.5kV/900A)

excellent performance

high reliability

Expected long lifetime

Introduction(Comparison of Conventional product and new product)

	CM750HG-130R (Conventional)	CM900HG-130X (New)
		
Package size	190 * 140 * 48mm	←
V_{CES}	6.5kV	←
I_C	750A	**900A**
$T_{jop(Max)}$	125°C	**150°C**

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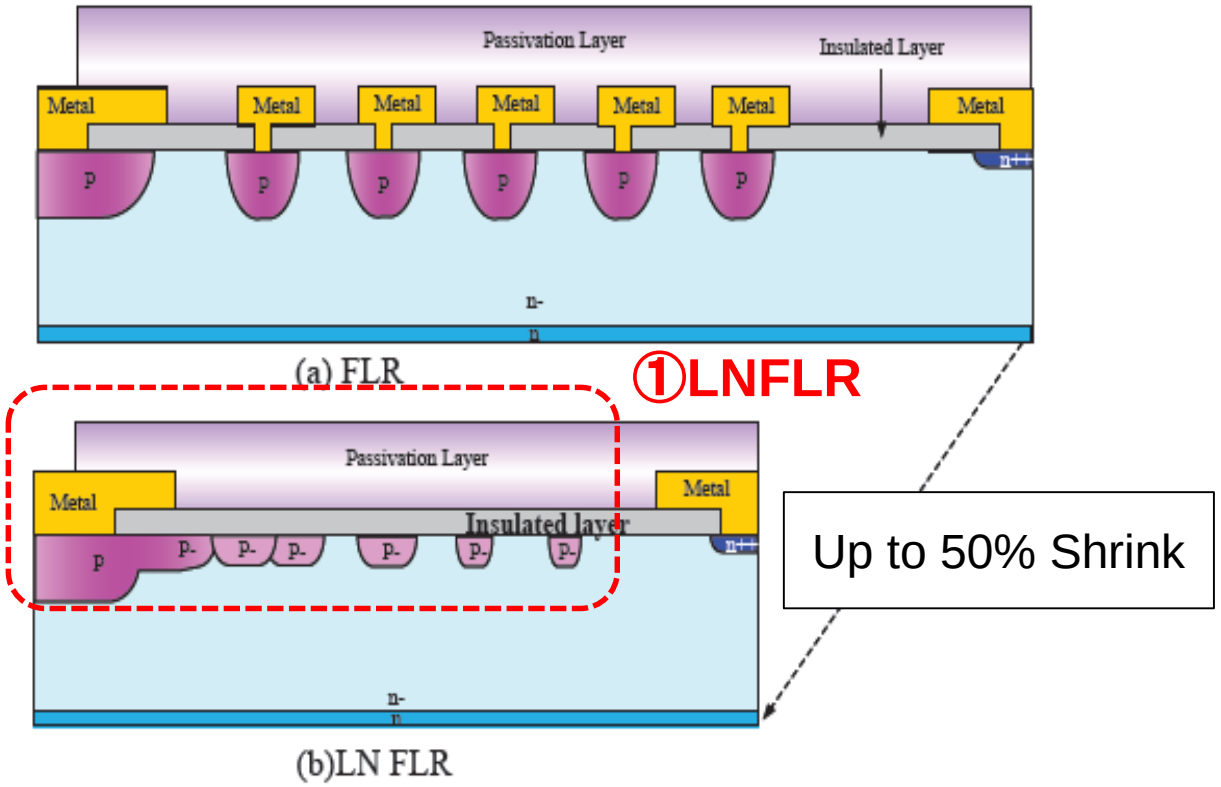
LNFLR for expansion of active area

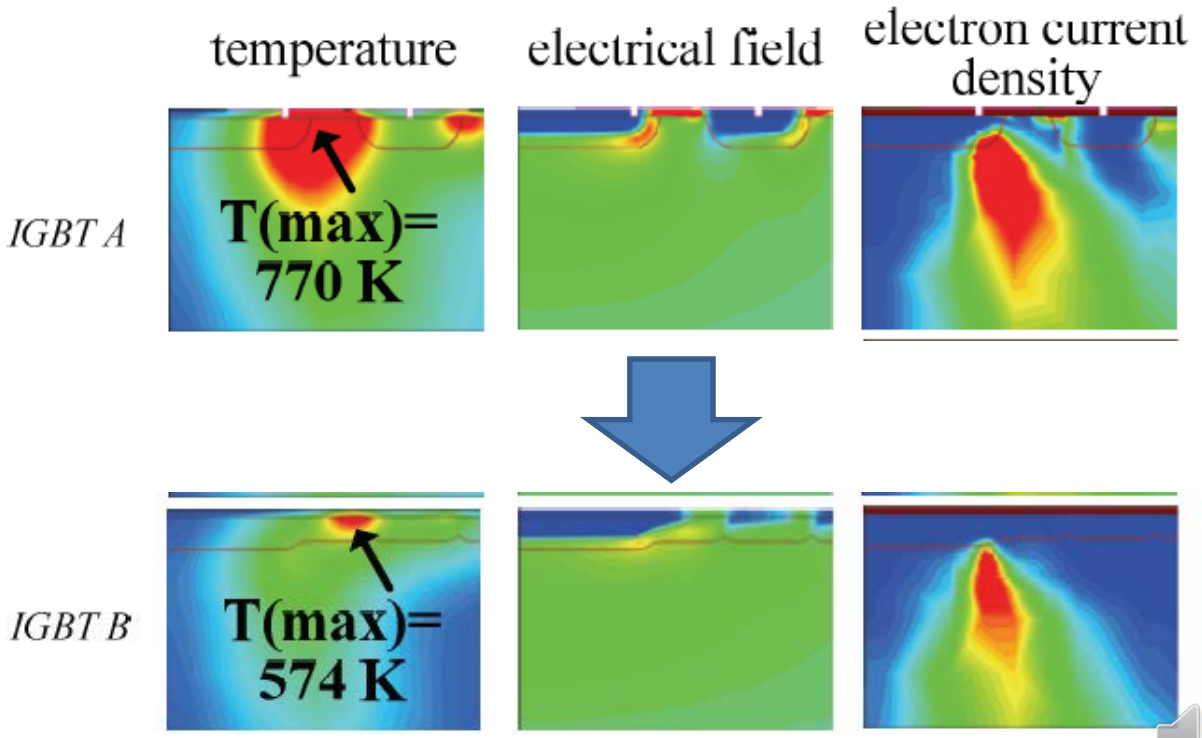
LNFLR: Linearly-Narrowed Field Limiting Ring

FLR→LNFLR

・It is Capable of shrinking the edge termination width by 50% without deteriorating the device's blocking capability and dynamic ruggedness.

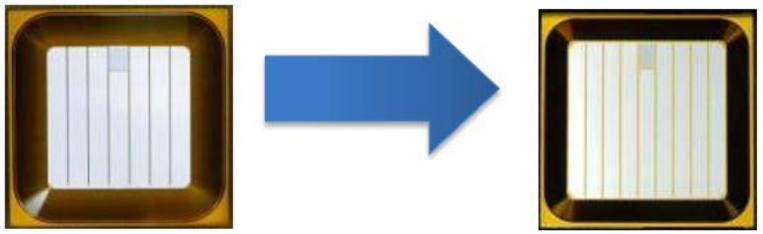
・It relaxes the electric field of the PN junction and lowers the maximum temperature of the IGBT from 770K to 574K.



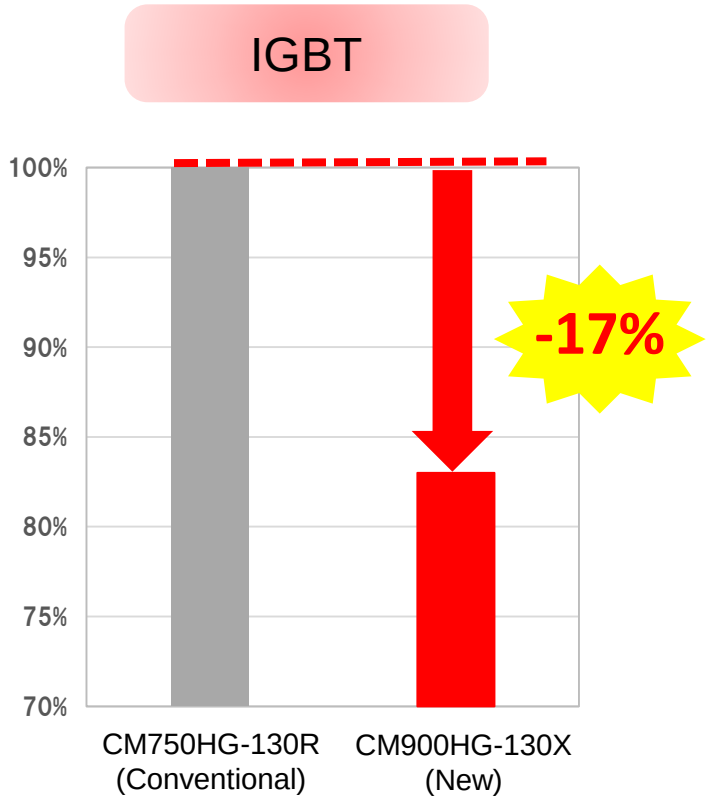


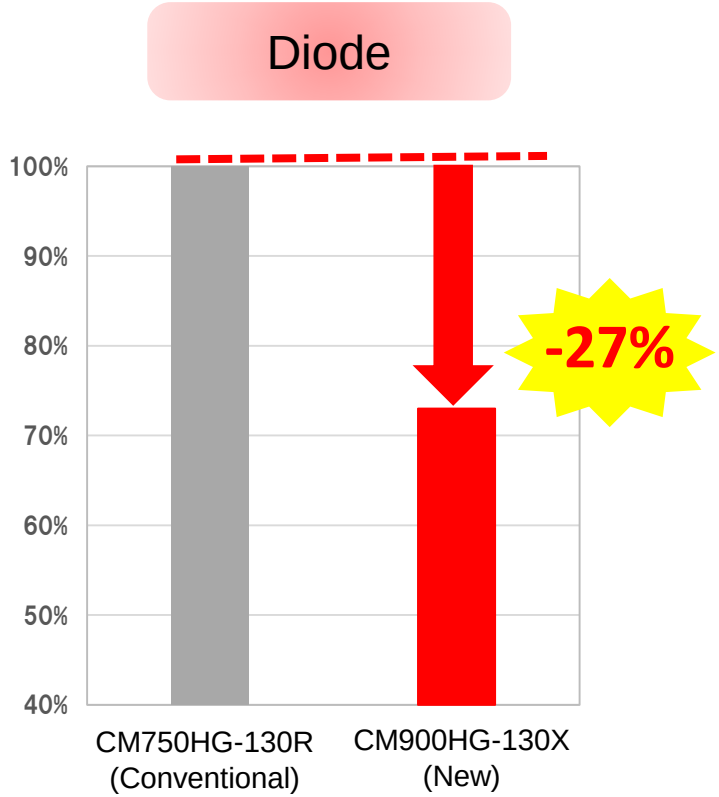
LNFLR for expansion of active area

LNFLR: Linearly-Narrowed Field Limiting Ring



Active area 28%up





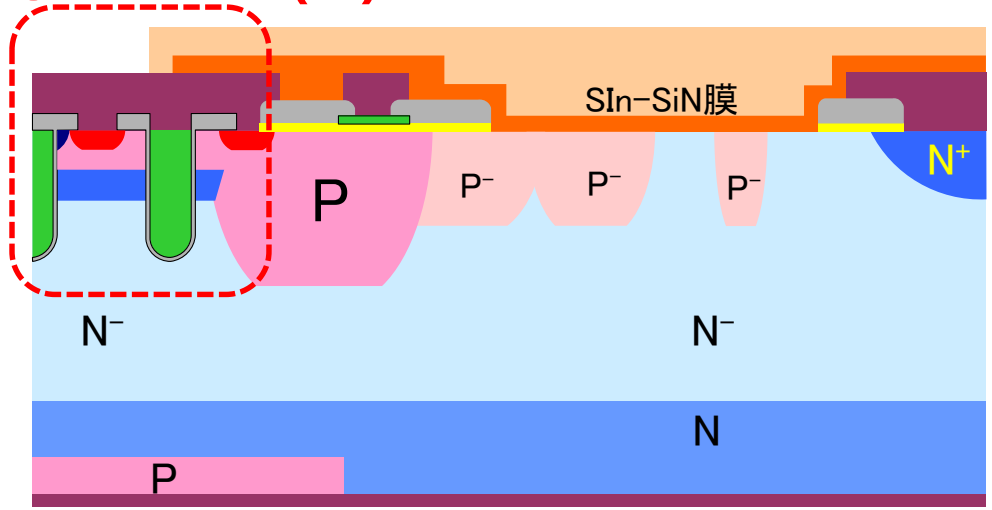
R_{th} of IGBT is reduced by 17% and R_{th} of diode is reduced by 27% by optimizing chip edge termination

CSTBT™ (III) for reduction of energy loss

CSTBT: Carrier Stored Trench Gate Bipolar Transistor

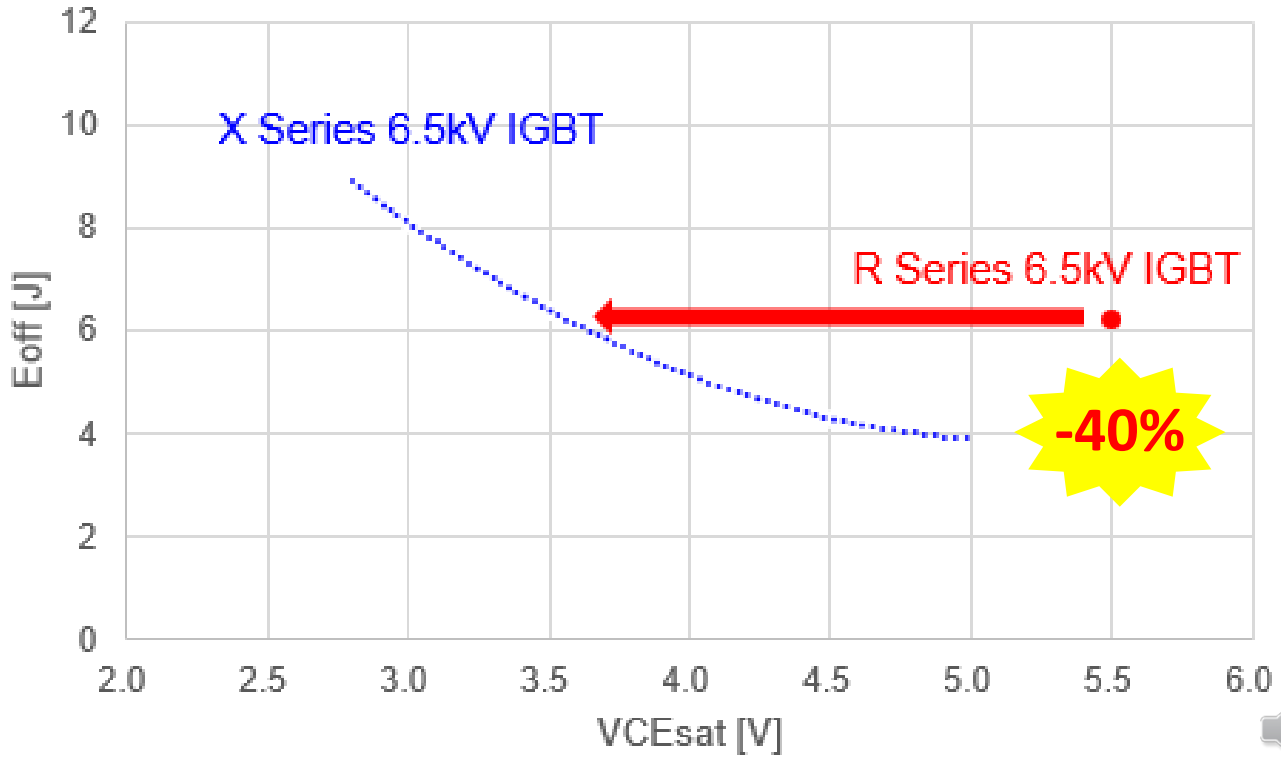
・CSTBT™ (III) can improve the trade-off between conduction loss and switching loss by the effect of the trench structure and carrier storage layer.
・It reduces V_{CEsat} by 40% with the same E_{off} compared to the conventional product.

②CSTBT™(Ⅲ)



Inverter losses reduction
New trench gate structure
→ CSTBT™ (III)
- Higher carrier concentration at emitter side under on-state

→ Lower V_{CEsat}



Partial P Collector for high robustness

- The maximum operating temperature of the X-series 6.5kV/900A HVIGBT is designed at 150 °C.
- npn transistor, the field failure rate become 1.37 times if use temperature rises 125°C to 150°C(MIL standard).
- Design margin against high temperature on a semiconductor device is important.

FIT rate is calculated according to MIL-HDBK-217F standard

Tj	Vcc	Ic_{RMS}	fc	Pr	λb	πT	πA	πR	πS	πQ	πE	**λP x 10^3[FIT]**
125	3600	450	150	1118	7.4.E-04	5.94	0.7	13.4	0.251	1	9	**93**
150	3600	450	150	1118	7.4.E-04	8.14	0.7	13.4	0.251	1	9	**128**

1.37 times

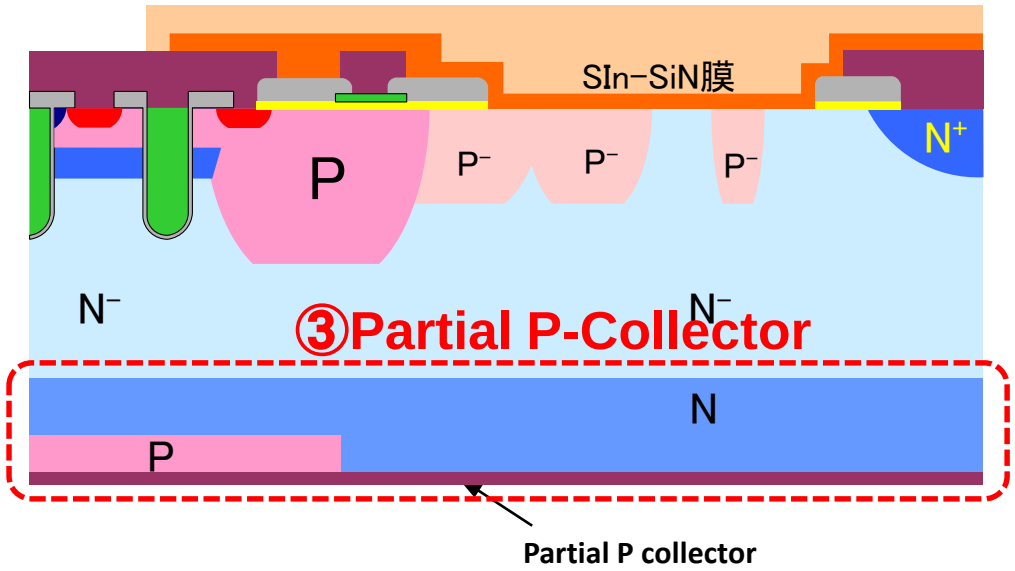
The detail calculation formula of FIT rate:

Category: Transistors, Low frequency (< 200MHz), Bipolar (NPN)

$\lambda_P = \lambda_b \times \pi_T \times \pi_A \times \pi_R \times \pi_S \times \pi_Q \times \pi_E$ [Failures/10^6 Hours]
λ_b = NPN basic failure rate
π_T = Temperature factor, "= exp[-2114(1/Tj+273 – 1/298)]"
π_A = Application factor, "switching" operation = 0.7
π_R = Power rating factor, "$(Pr)^{0.37}$" (Pr = inverter power loss calculation results by MelcoSim)
π_S = Voltage stress factor, "Vcc / Vces"
π_Q = Quality factor, "JANTX" = 1.0
π_E = Environment factor, "G_M: for transport" = 9.0, "N_S: for Power Transmission = 9.0"

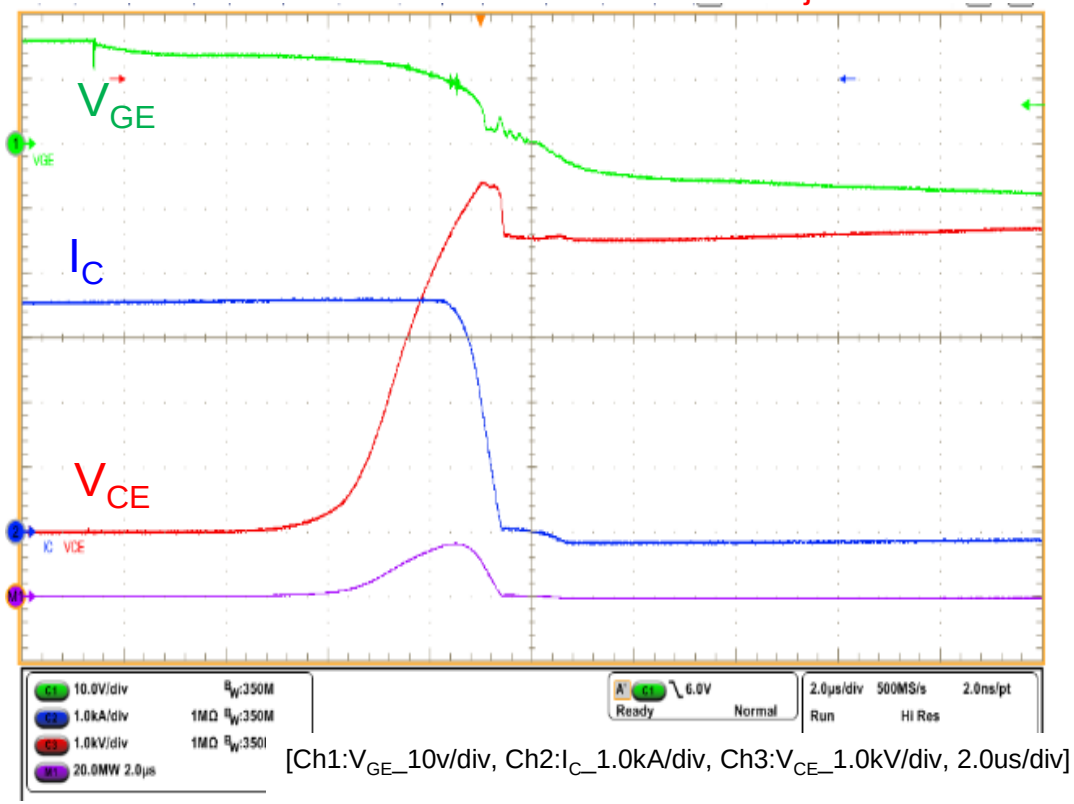
Partial P Collector for high robustness

- Pirtial P Collector provides sufficient margin for deterioration and failure due to turn-off switching even at high temperatures
- It can successfully turn off switching at Tj = 150 ºC, I_C = 3600 A (4.0x IC(nom)).



Wide SOA margin
→ Partial P collector
- Minimize hole injection efficiency in edge termination

I_C = 3600 A(4I_C), V_{CC} = 4500 V, T_j = 150 ºC



[Ch1:V_{GE}_10v/div, Ch2:I_C_1.0kA/div, Ch3:V_{CE}_1.0kV/div, 2.0us/div]

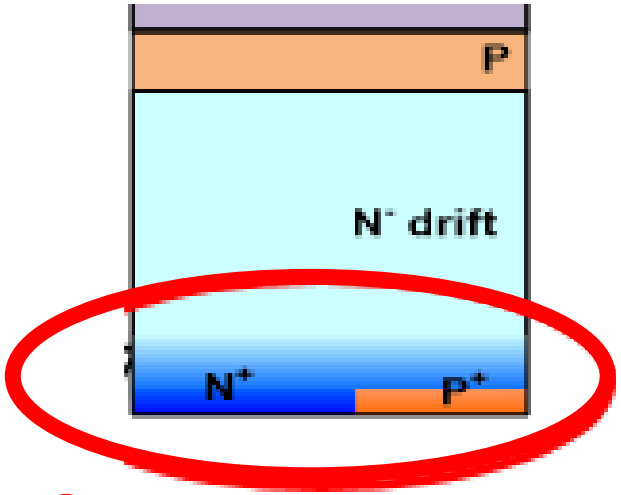
Turn-off switching waveform

Shota Saito

RFC for high robustness

RFC: Relaxed Field of Cathode

- RFC provides sufficient margin for deterioration and failure due to reverse recovery even at high temperatures
- It can smoothly reverse recovery without snap-off behavior, at Tj = 150 ºC.



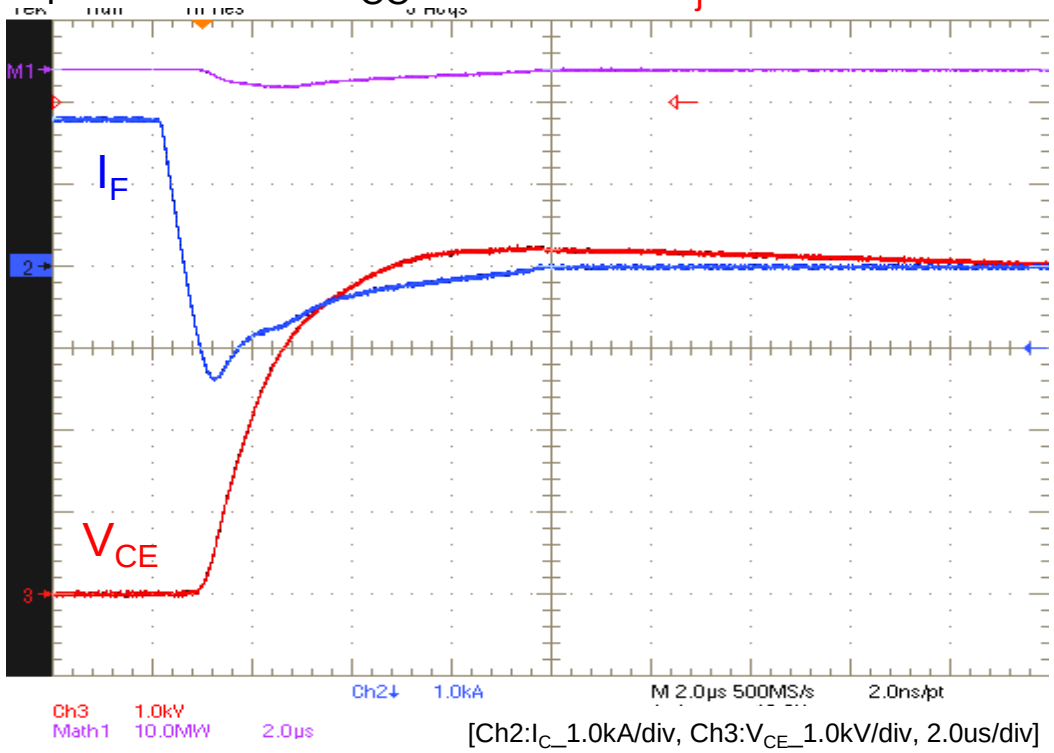
④RFC

Wide SOA margin

→ RFC

- electric field on the cathode side is relaxation by alternately using P and N layers on the back surface

I_F = 1800 A, V_{CC} = 4500 V, T_j = 150 ºC



[Ch2:I_C_1.0kA/div, Ch3:V_{CE}_1.0kV/div, 2.0us/div]

Reverse recovery waveform

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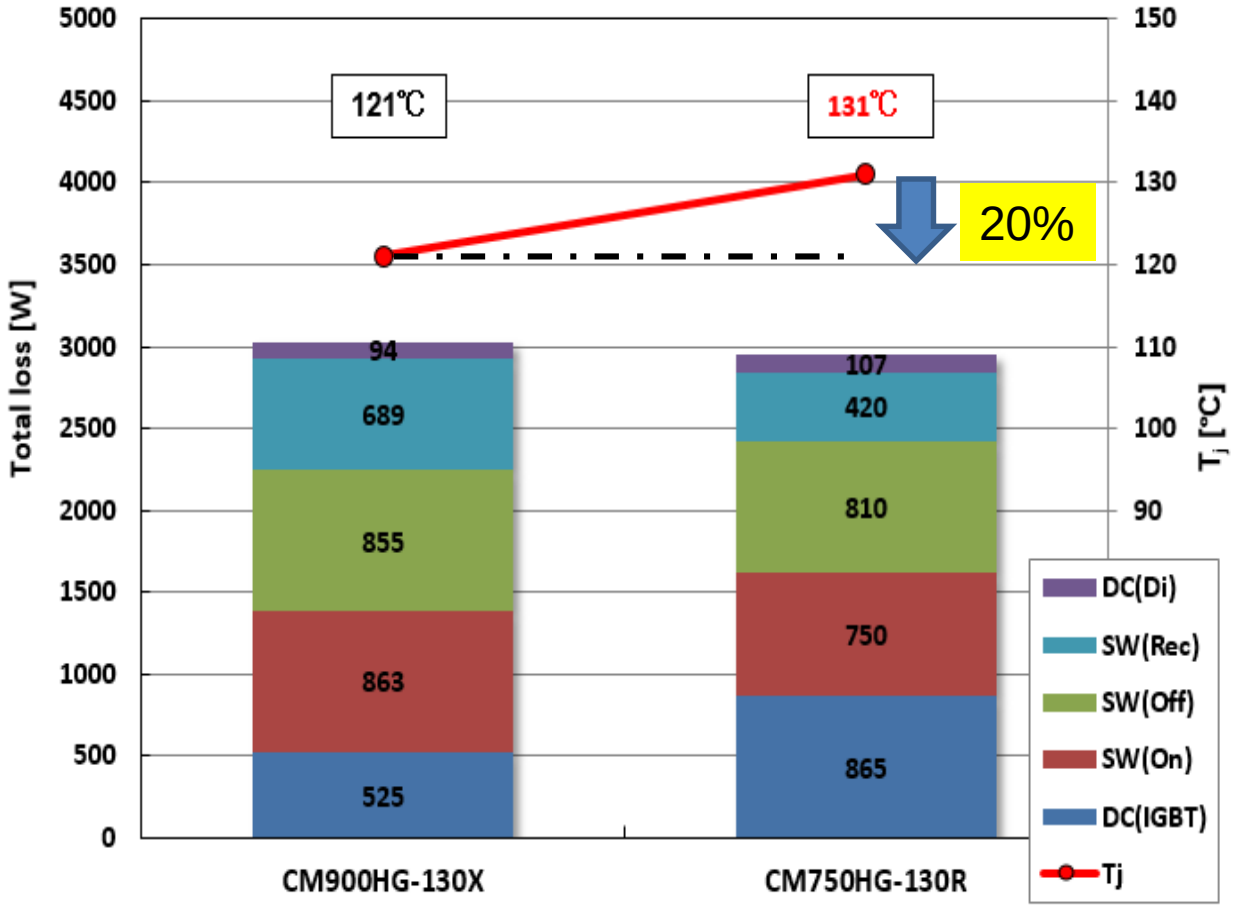
Cooling fin

Condition: V_{CC}=3600V, I_O=750Apeak, f_C=500 Hz, Modulation ratio＝1, f_O=50Hz, P.F=+0.85, T_S=80°C



Power loss simlaton

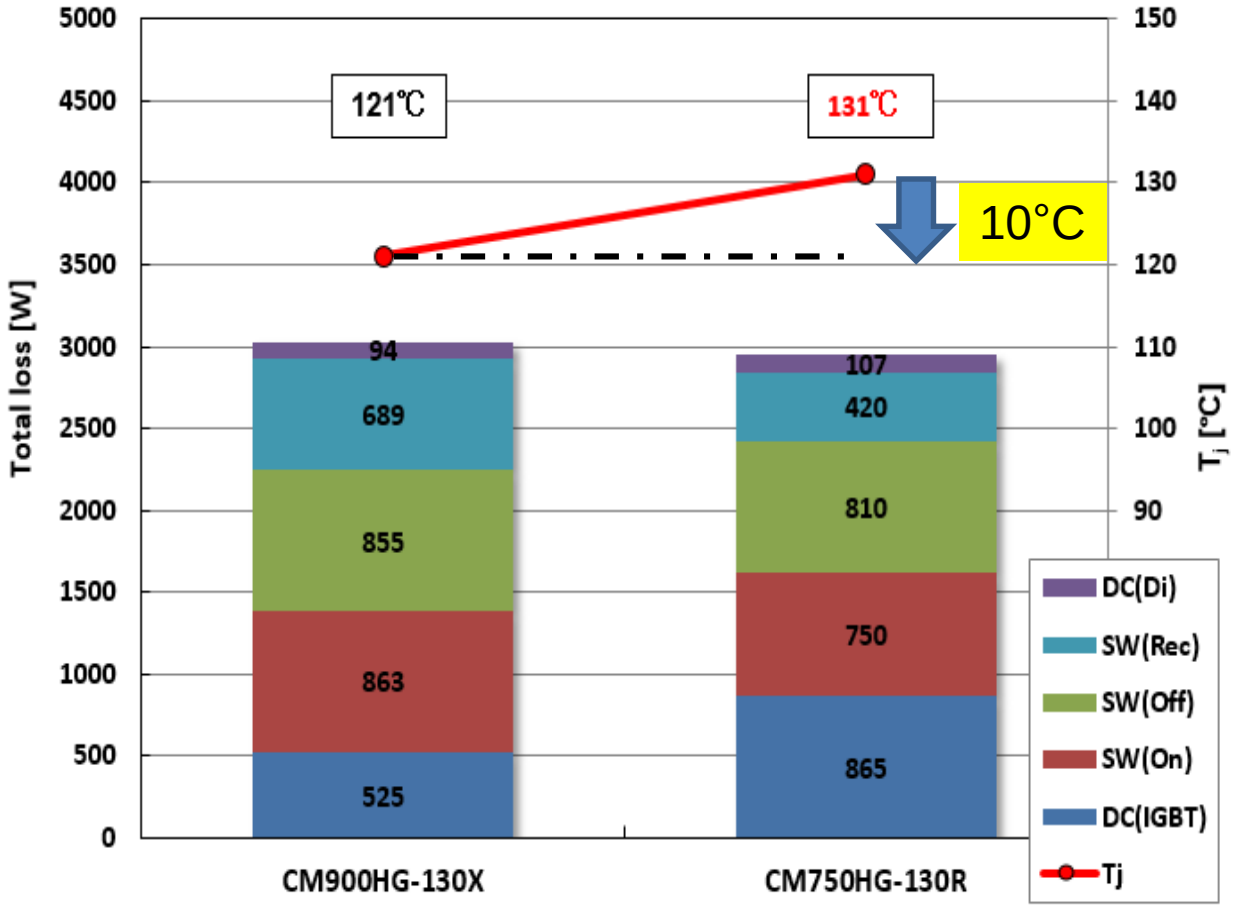
T_j reduced 20%.

cooling fins can be reduced by 20%*.

*Tresistance of the power semiconductor product and that of the radiatrion fin are 1:1

Reduce FIT rate

Condition: V_{CC}=3600V, I_O=750Apeak, f_C=500 Hz, Modulation ratio＝1, f_O=50Hz, P.F=+0.85, T_S=80°C



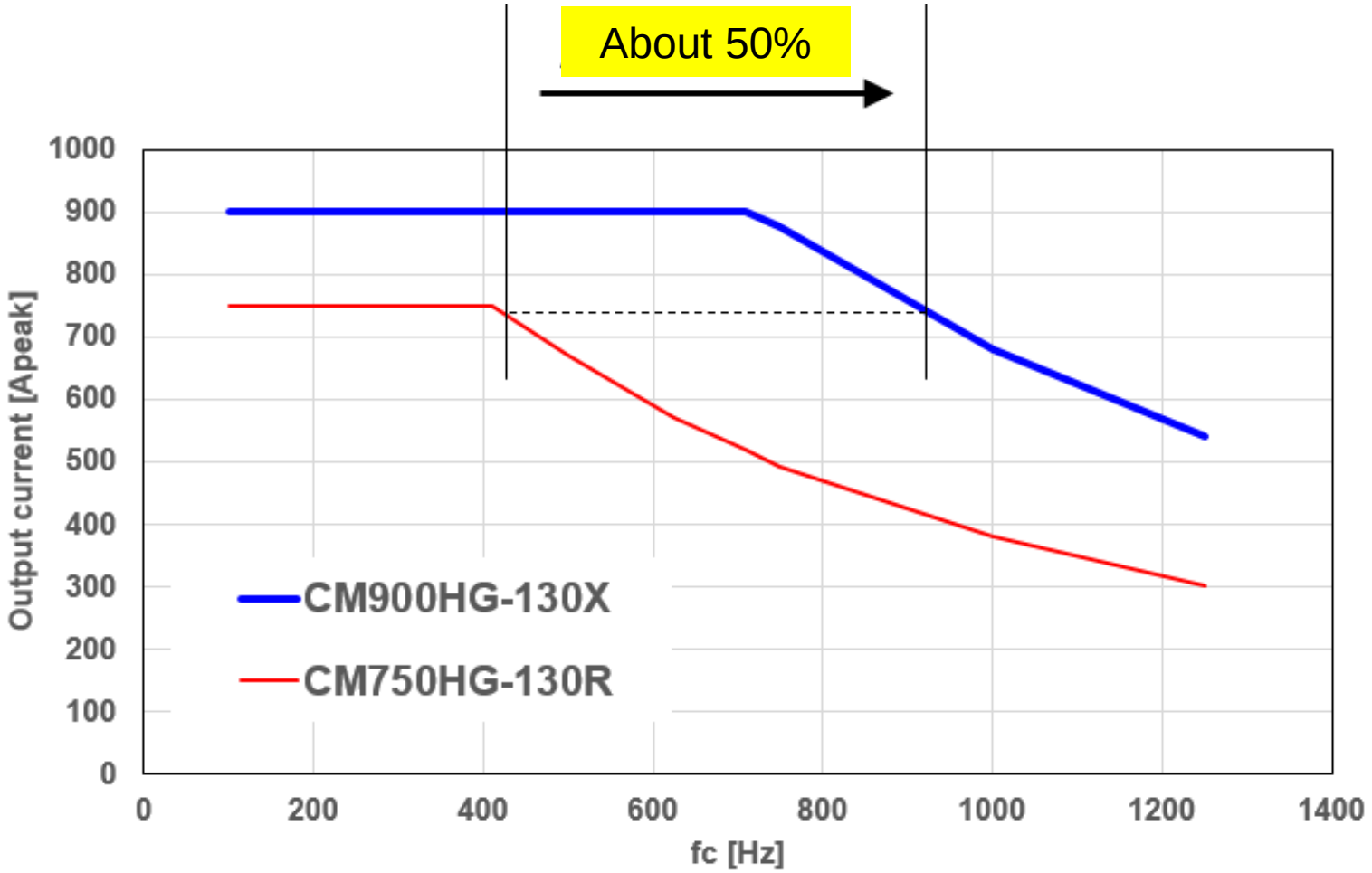
Power loss simlaton

T_j reduced 10°C.

failure rate is improved by about 15%*

*MIL standard.

Improving inverter efficiency by expanding the frequency range



Maximum carrier frequency increased by 50%

increases the motor efficiency by reducing motor loss and harmonic noise.

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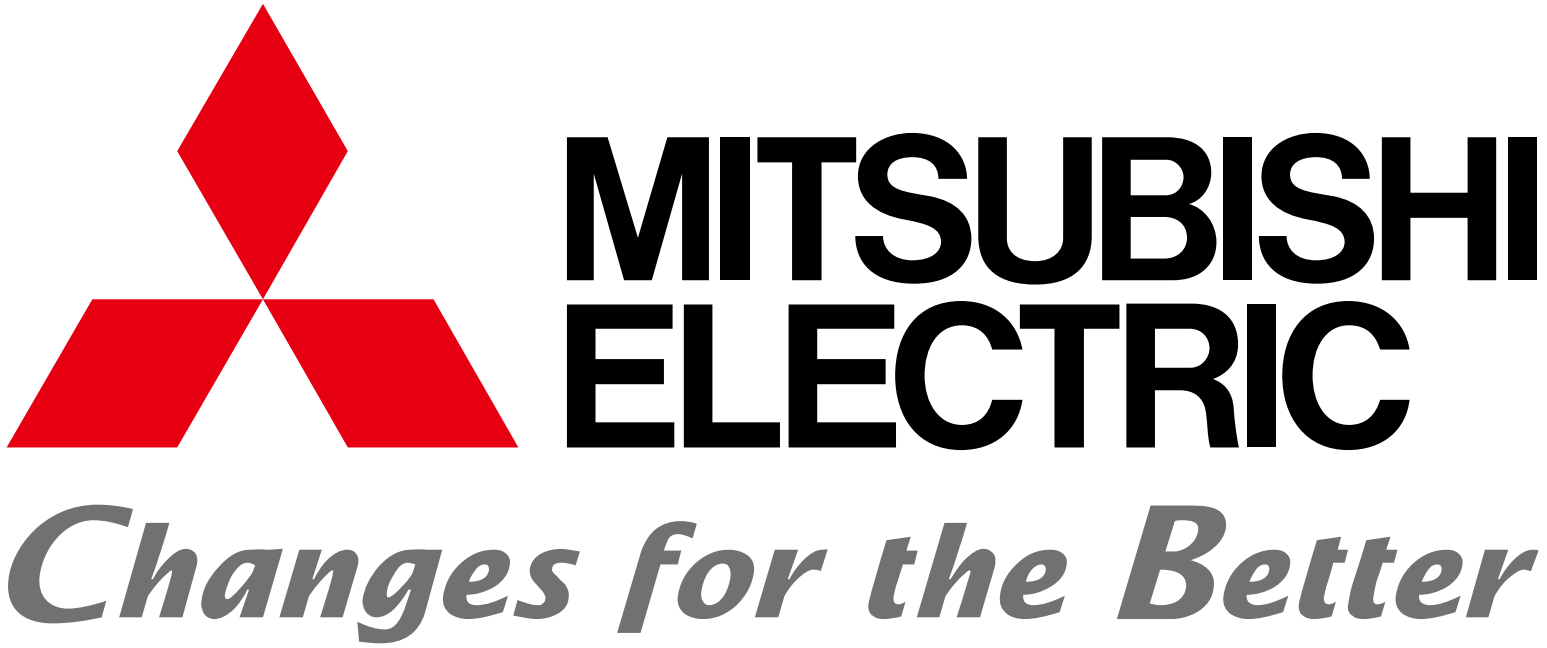
Conclusion

With chip technology of CM900HG-130X

- **Excellent performance**
  - 40% reduction in conduction loss
  - the improvement of the thermal resistance for IGBT part by 17% and Diode part by 27%
- **high reliability**
  - Successful turn-off switching and reverse recovery at maximum rated conditions of 150° C.
- **Expected long lifetime**
  - By replacing the conventional product, the temperature rise can be suppressed and the failure rate can be reduced by 15%.

1) Smaller size of power electronics equipment by optimizing the performance of the cooling fin.
2) Reduction of the maintenance cost by reducing the field failure rate by 15% or more.
3) Improvement of the efficiency for power electronics equipment by increasing the carrier frequency.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